Biasing LDMOS FETs for Linear Operation

Bias choices determine linearity, gain and efficiency, but also require attention to thermal effects

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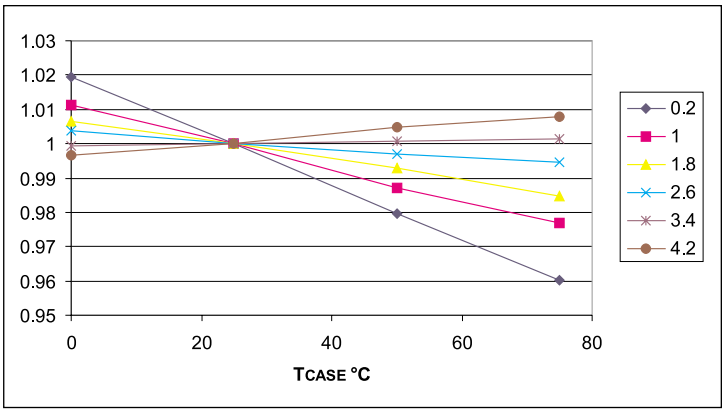
The new CDMA and WCDMA wireless standards have dramatically impacted the optimization criteria that a wireless base station designer might choose in designing or selecting RF ower amplifiers. Now, more than ever before, linearity is of paramount importance. Lateral DMOS devices have provided superior performance at a reasonable price per watt. RF power amplifier designers must choose the bias point that will give them the best trade-offs between linearity, gain and efficiency. In order to provide these high degrees of linearity under all reasonable conditions, this bias point must be reasonably maintained over time and temperature.



▲ **Figure 1. A standard typical temperature plot given by most manufacturers of commercial LDMOS devices.**

A FET device has three parameters that change with increasing temperature: the gate threshold shifts; g_m drops; and R_{DS} (on) goes down. The combined result of this is shown in Figure 1, displaying a standard typical temperature plot given by most manufacturers of commercial LDMOS devices. The gate bias values shown are normalized to 1 volt at 25° C and depict the bias values needed to maintain the graphed current point over temperature.

At low drain currents, the LDMOS device has a positive temperature coefficient. As the drain current increases, the positive coefficient becomes progressively less positive, until at very high currents it goes negative. This is wonderful protection against thermal runaway, but it makes the designer's job a little more difficult. These plots serve as a good basic guideline, but the designer should be aware that normal process variations might affect these curves slightly.

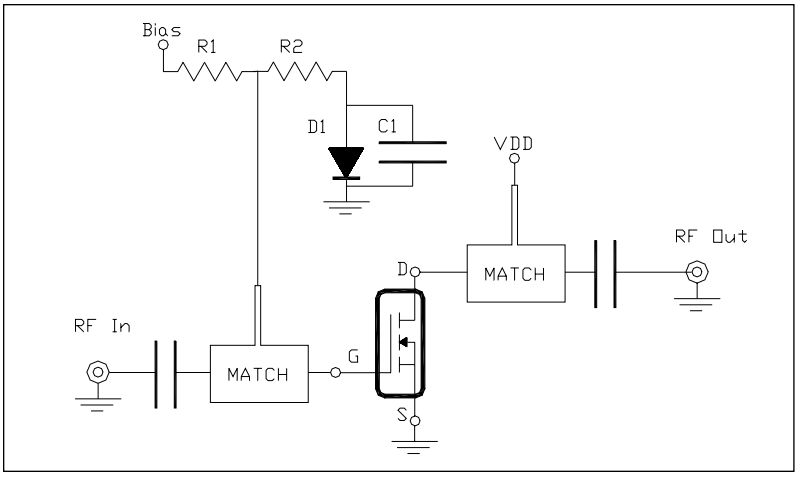
Basic considerations

In all FET bias circuits, it is of critical importance that the gate bias voltage be derived from a very well regulated source. It is also assumed that whatever sense element is used should be thermally linked to the device for which it is providing the correction reference. With the low currents present in the gate circuitry, this can be accomplished simply and very inexpensively. Furthermore, in linear operation, any "corrective" bias circuit will reduce the bias voltage with temperature to retain the same operating point. While at the same time g_m is dropping, this will appear as less amplifier gain at high temperatures. For most applications the gain change is slight, and most system designers provide a system ALC loop, which should mask this effect in the end product.

The diode compensation network

Diode compensation networks (as shown in

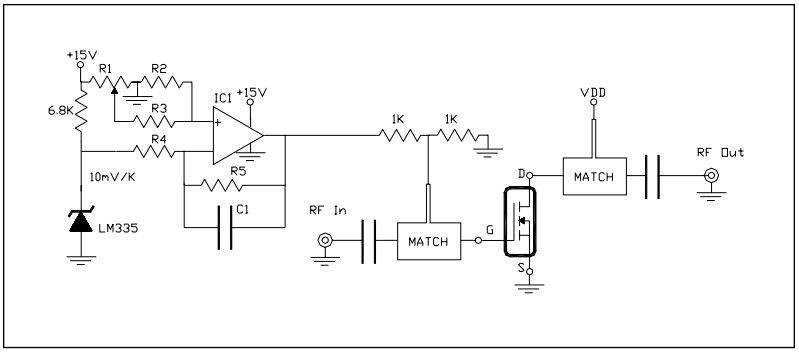
Figure 2) are perhaps the simplest and most widely used bias circuit. They have been used for years in bipolar circuits to prevent thermal runaway. There are excellent application articles available for their use in FET products as well. Operation is very straightforward. As D1 becomes hotter, its enhanced conduction will increase the current through R2, thus altering the divide ratio of R1/R2/D1. Single diode networks are, however, somewhat limited, in that it is more difficult to tailor the compensation curve to a specific device curve without additional circuitry. One may also series two or more diodes to increase the amount of compensation available.



▲ **Figure 2. Diode compensation network.**

The thermal sensor

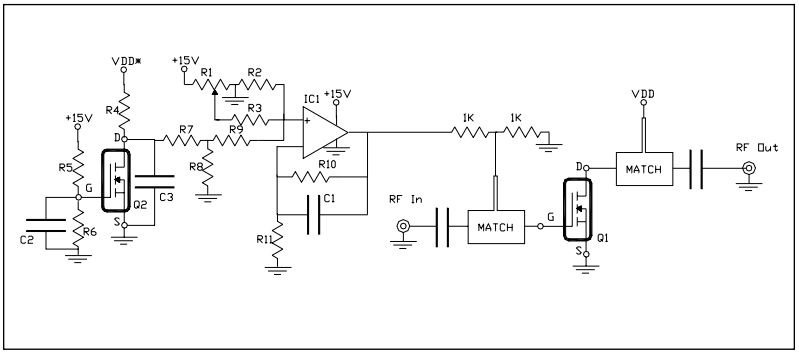
If the designer desires a bit more sophistication, a thermal sensor (as shown in Figure 3) may be used. This eliminates the guesswork and extra characterization associated with the diode compensator. The designer simply looks up the thermal coefficient of the device at the specific desired operating current, then compares that to the 10 mV/K slope of the temperature sensor (in this case, LM335). A simple op-amp circuit takes care of providing the desired slope conversion. In the sensor shown in Figure 3, R1 can be replaced by automated methods of main bias control for the device (e.g., I_{DQ} set from the system controller). R4 will adjust the amount of temperature slope at the output of IC1. R2, R3, and R5 may be tailored to the bias controls of individual systems. This is a well behaved configuration that is easily modeled in Spice.



▲ **Figure 3. Thermal sensor.**

The "Like material" reference

When the designer wants the mirroring effect in a compensation circuit as close to perfect as possible, there is no substitute for a "like material" reference (as shown in Figure 4). Q2 contains an RF transistor die that is similar in semiconductor processing characteristics to the die contained in Q1, but is much smaller (for this discussion, 1/56 size). Q2 is kept small to maximize system efficiency. The reference device may be any scalable size. R5 and R6 set the gate bias on Q2, typically set so that the drain current is scaled down to the same ratio as the difference in die size. For example, if the normal operating current in Q1 is 2.6 amperes, Q2 would be set to run at 1/56 of that value (assuming a 56:1 Q1/Q2 size ratio). As Q2 changes temperature, the change in current causes the drain voltage of Q2 to change. This voltage feeds the correction input of the op-amp Summing circuit above.



▲ **Figure 4. "Like material" reference.**

A second, less obvious advantage to this topology is compensation for hot electron effects. High frequency (short gate length) lateral DMOS devices exhibit over time a gate oxide charging phenomenon. This oxide charging leads to an upward shift in threshold voltage in the enhancement mode device. For example, assume that the gate bias of an FET is set so that the quiescent drain current is 1 A. If the FET is operated for 20 years and the quiescent current is re-measured as 0.95 A, the FET has drifted 5 percent, due to this oxide charging effect. One ampere was the value of quiescent current

that provided optimal linearity performance; consequently the linearity performance (and small signal gain) of our device has degraded over time. These effects are minimized if the gate bias is increased over time to compensate for the charging effect. In the ideal case, V_{DD}* will be above V_{DD} so that with the current drawn the actual V_{DD} of Q2 will approximate V_{DD} on Q1.

One very important assumption for this is that both transistors are "new" when installed. (On a mass production base station line, this will not be an issue.) When properly implemented, the "like material" reference compensates for many drift and thermal effects. This is certainly not a perfect solution, but it allows offsetting negative characteristics to subtract; even if material types are not perfectly matched, you are still subtracting errors.

Although device manufacturers are continually reducing this drift effect, it will be a factor for some time to come. The "like material" reference eliminates the need for burn in, but requires the amplifying and compensating devices be of identical "age." This may add substantial cost to any field replacement of devices.

The correction circuits presented here are generic in nature, and may be modified to individual system requirements. This paper is intended as a general reference only. Equations for the sum/difference circuits are available in the references. Most of these correction circuits are easily modeled. If a higher degree of manufacturing ease is needed a custom integrated circuit could be produced for method 1 or 2. ■

References

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